Index	Command	Command Code	Comments
1.	BYPASS	0_0000;	// Prior Art – Test BYPASS.
2.	SAMPLE	0_0001;	// Prior Art – Test Sample/Preload.
3.	EXTEST	0_0010;	// Prior Art – Test EXTEST.
4.	HIGHZ	0_0011;	// Prior Art – Test High impedance.
5.	CLAMP	0_0100;	// Prior Art – Test CLAMP.
6.	ID_CODE	0_0101;	// Prior Art – Test Identification code.
7.	RUN_SCAN	0_0110;	// Test scan cores.
8.	RUN_MBIST	0_0111;	// Test memory BIST cores.
9.	RUN_LBIST	0_1000;	// Test logic BIST cores.
10.	DBG_SCAN	1_0000;	// Debug scan cores.
11.	DBG_MBIST	1_0001;	// Debug memory BIST cores.
12.	DBG_LBIST	1_0010;	// Debug logic BIST cores.
13.	DBG_FUNCTION	1_0011;	// Debug functional cores.
14.	SELECT	1_0100 10010;	// Debug MBIST/LBIST cores 4 and 1.
15.	SHIFT	1_0101 0110_1100;	// Shift data in and out of scan cells.
16.	SHIFT_CHAIN	1_0110 2 1100;	// Shift data in and out of scan chain 2.
17.	CAPTURE	1_0111;	// Capture results to all scan cells.
18.	SKIP	1_1000 1_0000_0000;	// Skip errors for 64 <cycles>.
19.	RESET	1_1001;	// Reset the circuit under test.
20.	BREAK	1_1010 1 0000_0001_0000_0000;	// Stop when 1st break bus1 = 4h'0100.
21.	BREAK	1_1010 2 1001_0011_0110;	// Stop when 2nd break bus2 = 3h'936.
22.	RUN	1_1011;	// Run system clocks forever.
23.	STEP	1_1100 1_0000_0000;	// Run system clocks 64 <cycles>.
24.	STOP	1_1101;	// Stop system clocks.

FIG. 1

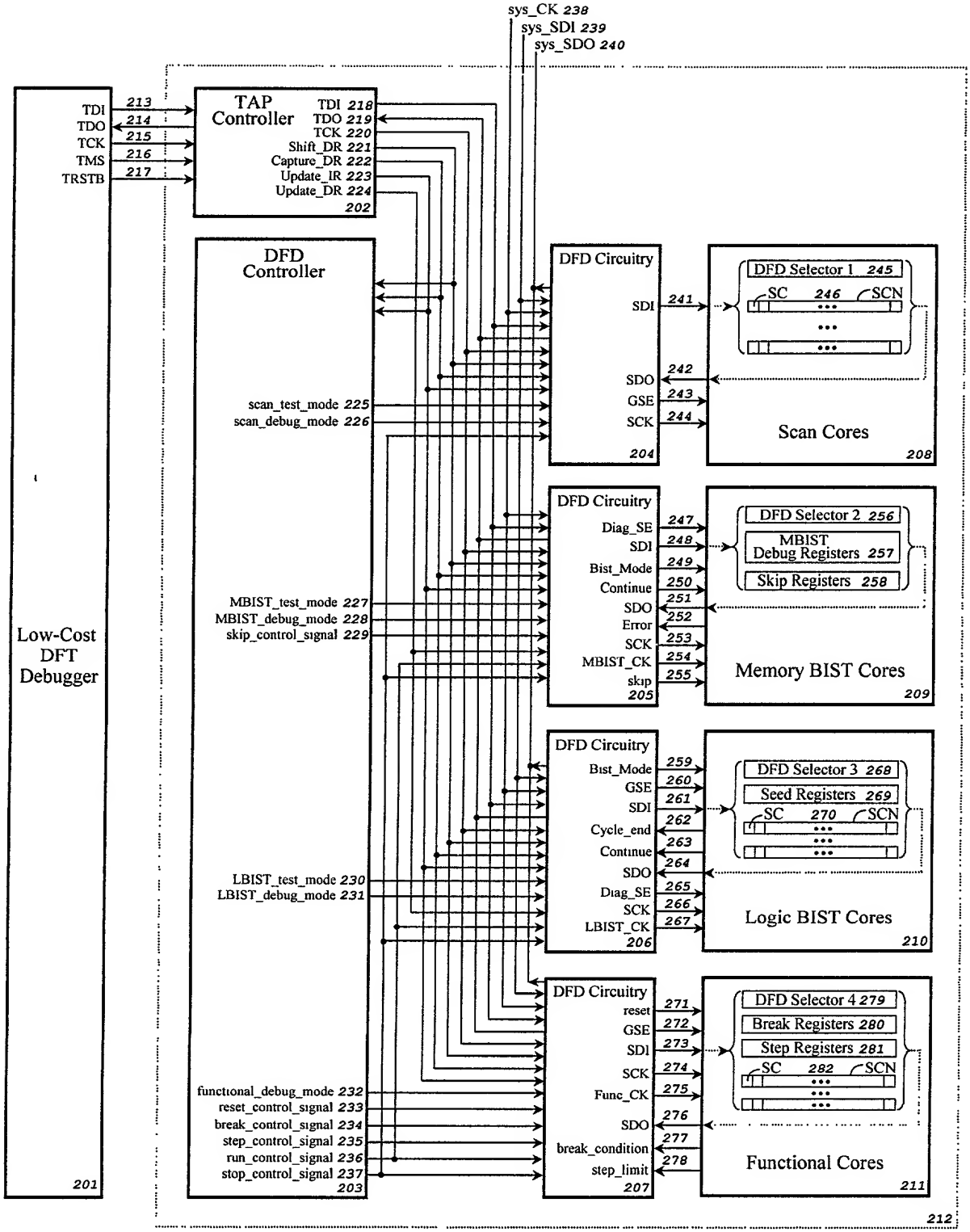

sys_CK 238
sys_SDI 239
sys_SDO 240
Low-Cost DFT Debugger
201
TDI 213
TDO 214
TCK 215
TMS 216
TRSTB 217
TAP Controller
TDI 218
TDO 219
TCK 220
Shift_DR 221
Capture_DR 222
Update_IR 223
Update_DR 224
202
DFD Controller
scan_test_mode 225
scan_debug_mode 226
MBIST_test_mode 227
MBIST_debug_mode 228
skip_control_signal 229
LBIST_test_mode 230
LBIST_debug_mode 231
functional_debug_mode 232
reset_control_signal 233
break_control_signal 234
step_control_signal 235
run_control_signal 236
stop_control_signal 237
203
DFD Circuitry
SDI 241
SDO 242
GSE 243
SCK 244
204
DFD Selector 1 245
SC 246
SCN
Scan Cores
208
DFD Circuitry
Diag_SE 247
SDI 248
Bist_Mode 249
Continue 250
SDO 251
Error 252
SCK 253
MBIST_CK 254
skip 255
205
DFD Selector 2 256
MBIST Debug Registers 257
Skip Registers 258
Memory BIST Cores
209
DFD Circuitry
Bist_Mode 259
GSE 260
SDI 261
Cycle_end 262
Continue 263
SDO 264
Diag_SE 265
SCK 266
LBIST_CK 267
206
DFD Selector 3 268
Seed Registers 269
SC 270
SCN
Logic BIST Cores
210
DFD Circuitry
reset 271
GSE 272
SDI 273
SCK 274
Func_CK 275
SDO 276
break_condition 277
step_limit 278
207
DFD Selector 4 279
Break Registers 280
Step Registers 281
SC 282
SCN
Functional Cores
211
212

FIG. 2

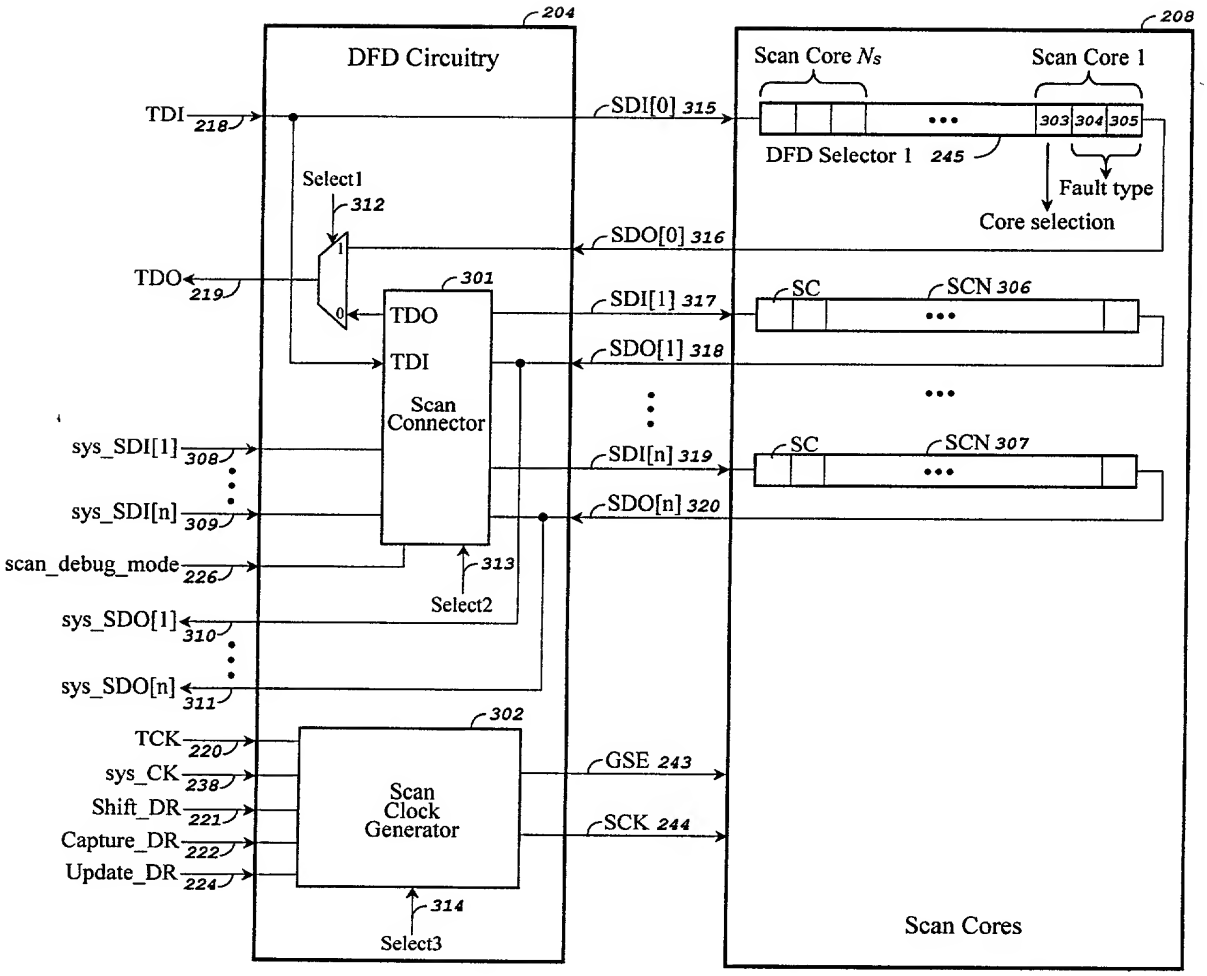

204
DFD Circuitry
208
Scan Core N_S
Scan Core 1
TDI 218
SDI[0] 315
303 304 305
DFD Selector 1 245
Fault type
Core selection
Select1 312
SDO[0] 316
TDO 219
301
TDO
TDI
Scan Connector
SDI[1] 317
SC
SCN 306
SDO[1] 318
SDI[n] 319
SC
SCN 307
SDO[n] 320
sys_SDI[1] 308
sys_SDI[n] 309
scan_debug_mode 226
313
Select2
sys_SDO[1] 310
sys_SDO[n] 311
302
TCK 220
sys_CK 238
Shift_DR 221
Capture_DR 222
Update_DR 224
Scan Clock Generator
GSE 243
SCK 244
314
Select3
Scan Cores

FIG. 3

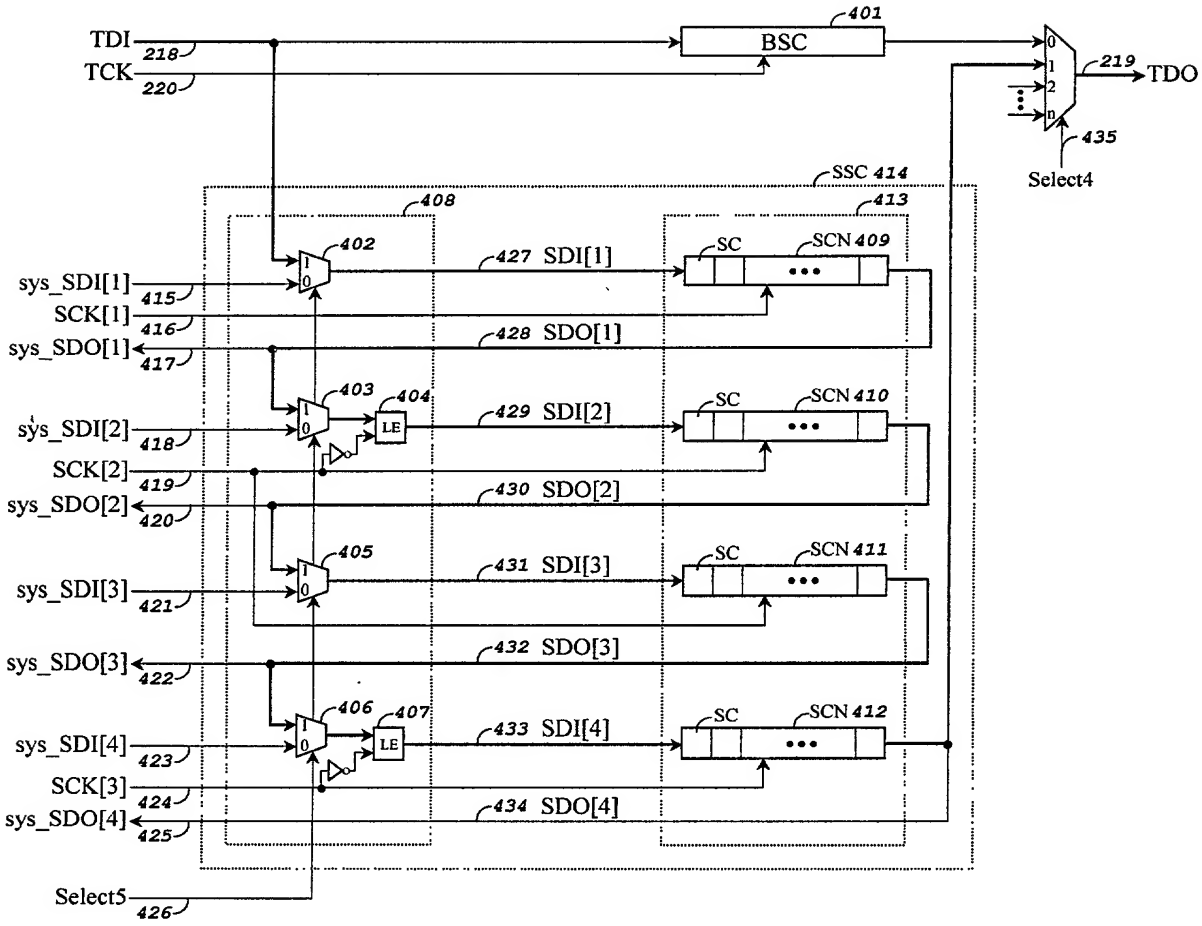
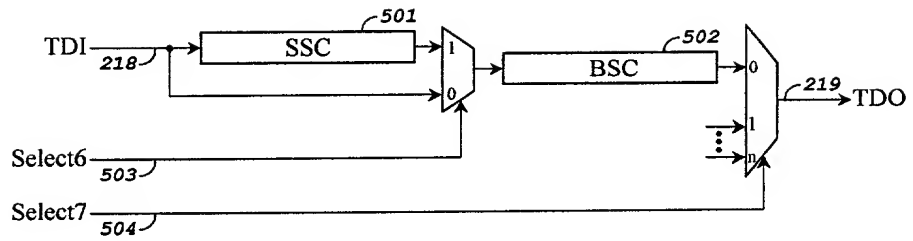
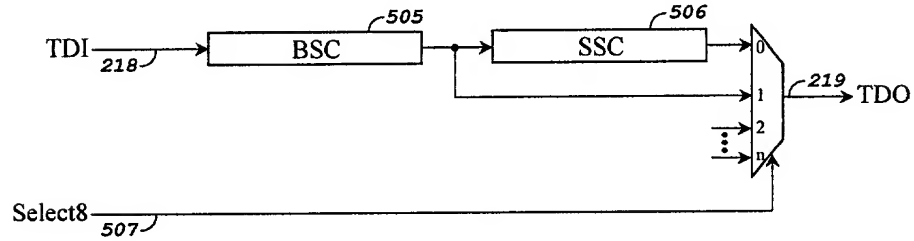

TDI
218
TCK
220
401
BSC
219
TDO
435
Select4
SSC 414
408
413
402
427 SDI[1]
SC
SCN 409
sys_SDI[1]
415
SCK[1]
416
sys_SDO[1]
417
428 SDO[1]
403
404
LE
429 SDI[2]
SC
SCN 410
sys_SDI[2]
418
SCK[2]
419
sys_SDO[2]
420
430 SDO[2]
405
431 SDI[3]
SC
SCN 411
sys_SDI[3]
421
sys_SDO[3]
422
432 SDO[3]
406
407
LE
433 SDI[4]
SC
SCN 412
sys_SDI[4]
423
SCK[3]
424
sys_SDO[4]
425
434 SDO[4]
Select5
426

FIG. 4


TDI
218
SSC
501
1
0
BSC
502
0
1
n
219
TDO
Select6
503
Select7
504

(a)


TDI
218
BSC
505
SSC
506
0
1
2
n
219
TDO
Select8
507

(b)

FIG. 5

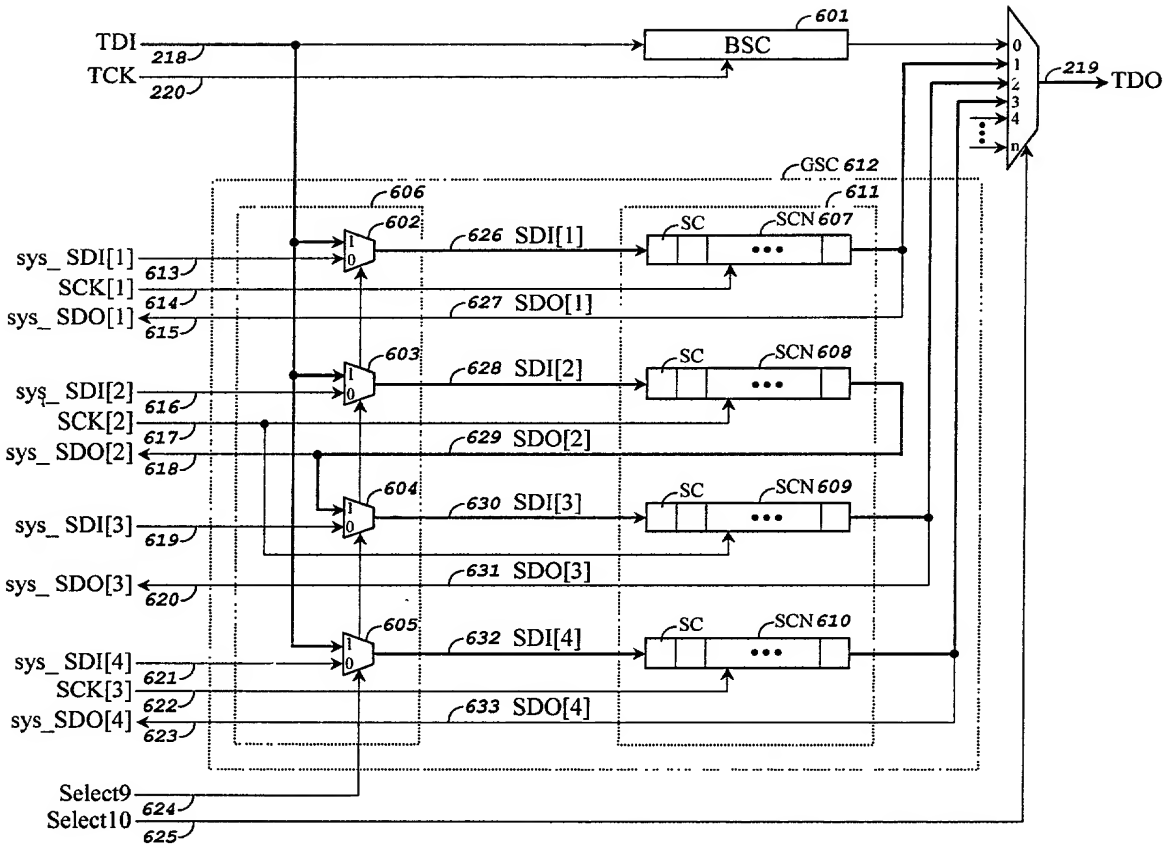
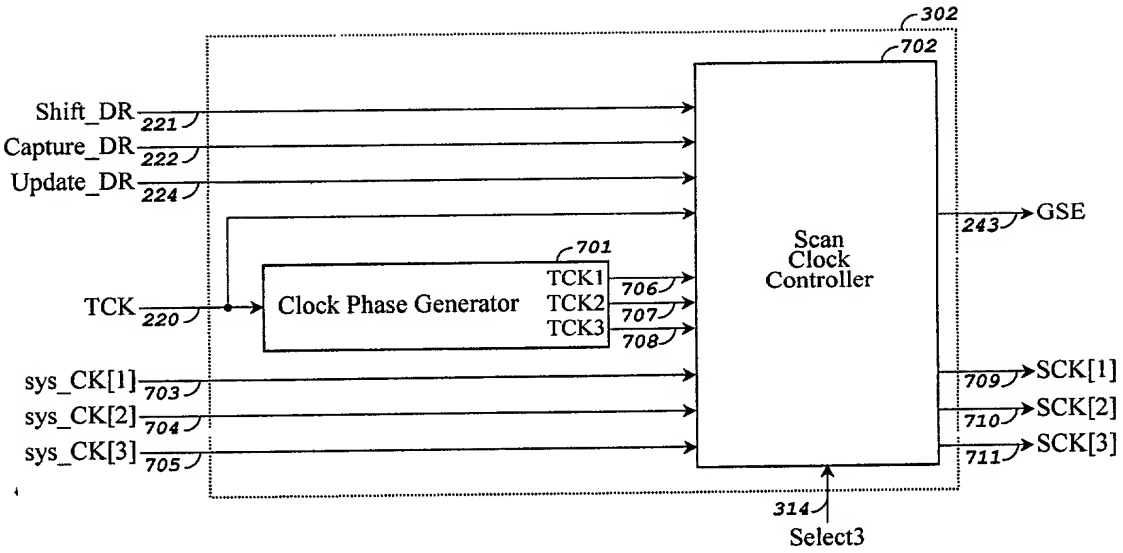
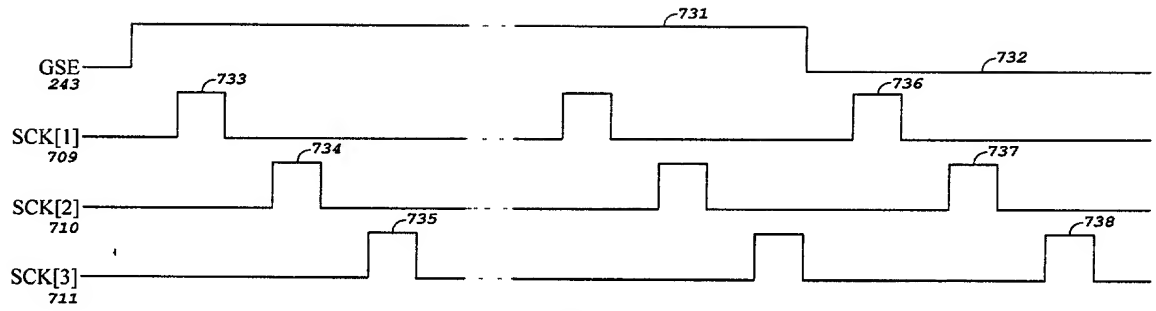

TDI
218
TCK
220
601
BSC
219
TDO
GSC 612
606
602
611
SC
SCN 607
sys_ SDI[1]
613
SCK[1]
614
sys_ SDO[1]
615
626 SDI[1]
627 SDO[1]
603
SCN 608
sys_ SDI[2]
616
SCK[2]
617
sys_ SDO[2]
618
628 SDI[2]
629 SDO[2]
604
SCN 609
sys_ SDI[3]
619
sys_ SDO[3]
620
630 SDI[3]
631 SDO[3]
605
SCN 610
sys_ SDI[4]
621
SCK[3]
622
sys_SDO[4]
623
632 SDI[4]
633 SDO[4]
Select9
624
Select10
625

FIG. 6

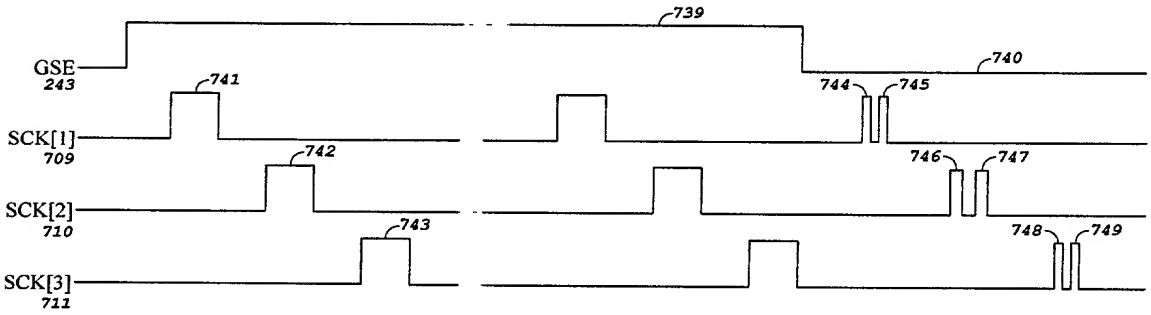


(a)

FIG. 7 Sheet-1

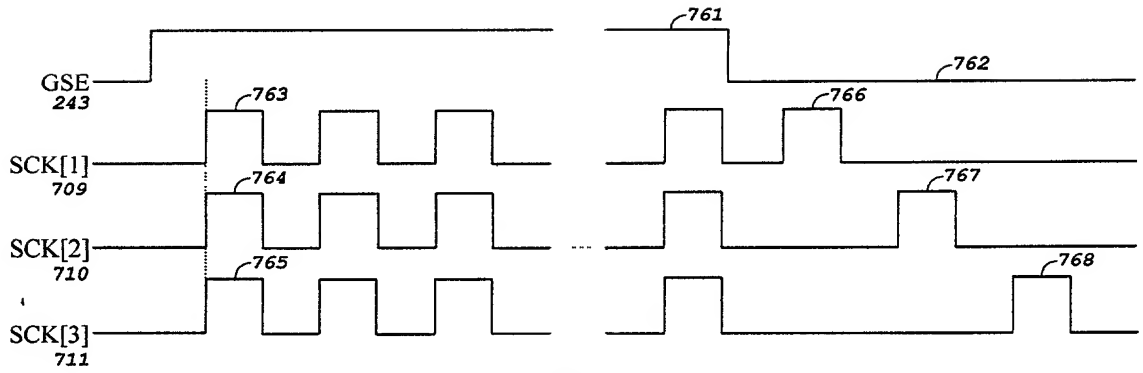


(b) Select3 = 0

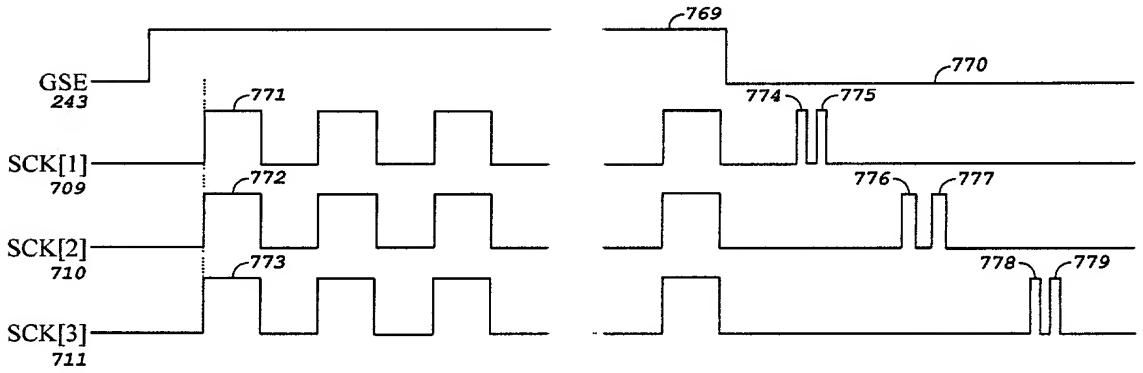


(c) Select3 = 1

FIG. 7 Sheet-2



(d) Select3 = 2



(e) Select3 = 3

FIG. 7 Sheet-3

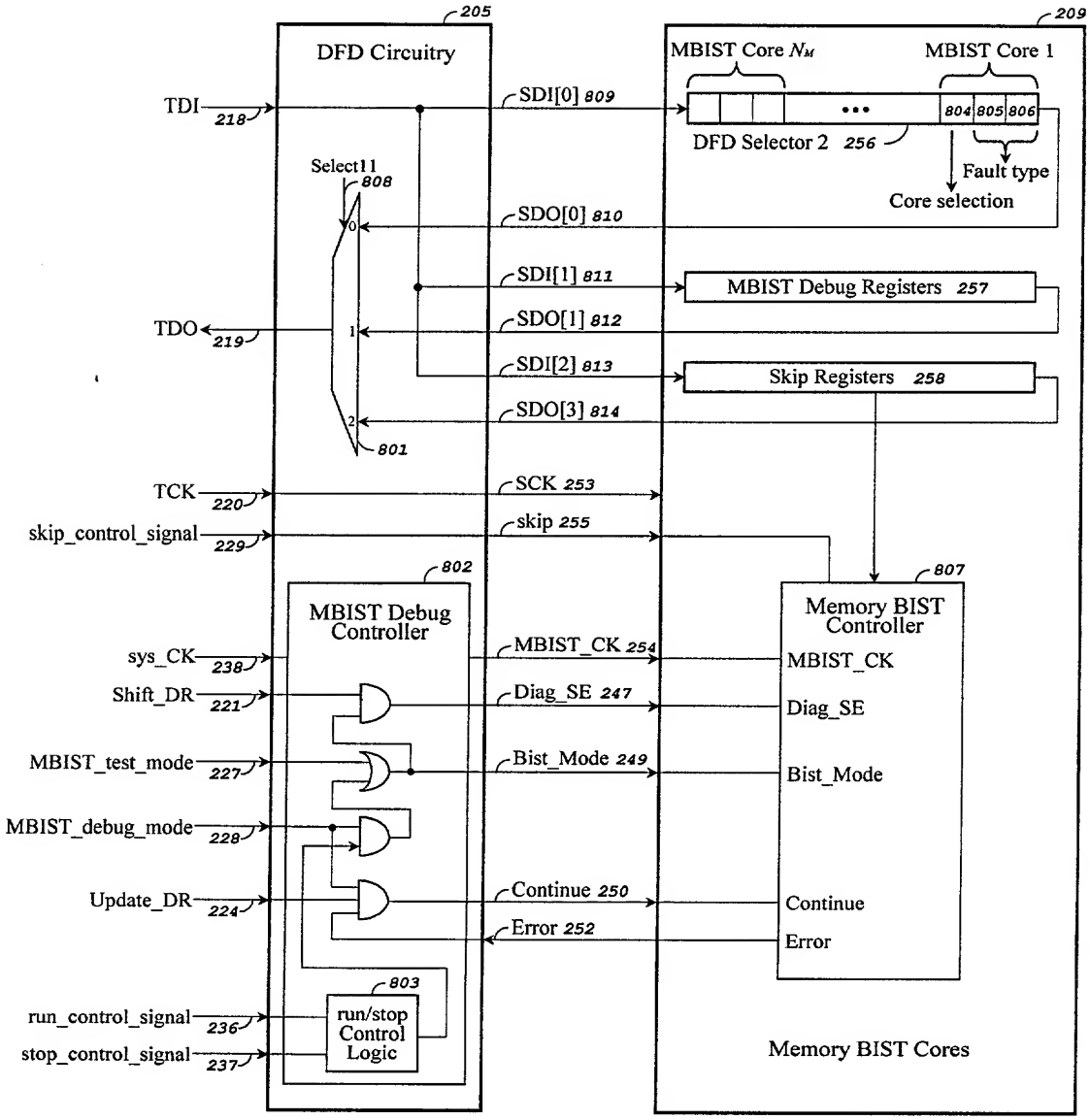

205
DFD Circuitry
209
MBIST Core N_M
MBIST Core 1
TDI
218
SDI[0] 809
804
805
806
DFD Selector 2 256
Fault type
Core selection
Select11
808
SDO[0] 810
SDI[1] 811
MBIST Debug Registers 257
TDO
219
SDO[1] 812
SDI[2] 813
Skip Registers 258
SDO[3] 814
801
TCK
220
SCK 253
skip_control_signal
229
skip 255
802
807
MBIST Debug Controller
Memory BIST Controller
sys_CK
238
MBIST_CK 254
MBIST_CK
Shift_DR
221
Diag_SE 247
Diag_SE
MBIST_test_mode
227
Bist_Mode 249
Bist_Mode
MBIST_debug_mode
228
Update_DR
224
Continue 250
Continue
Error 252
Error
803
run_control_signal
236
run/stop Control Logic
stop_control_signal
237
Memory BIST Cores

FIG. 8

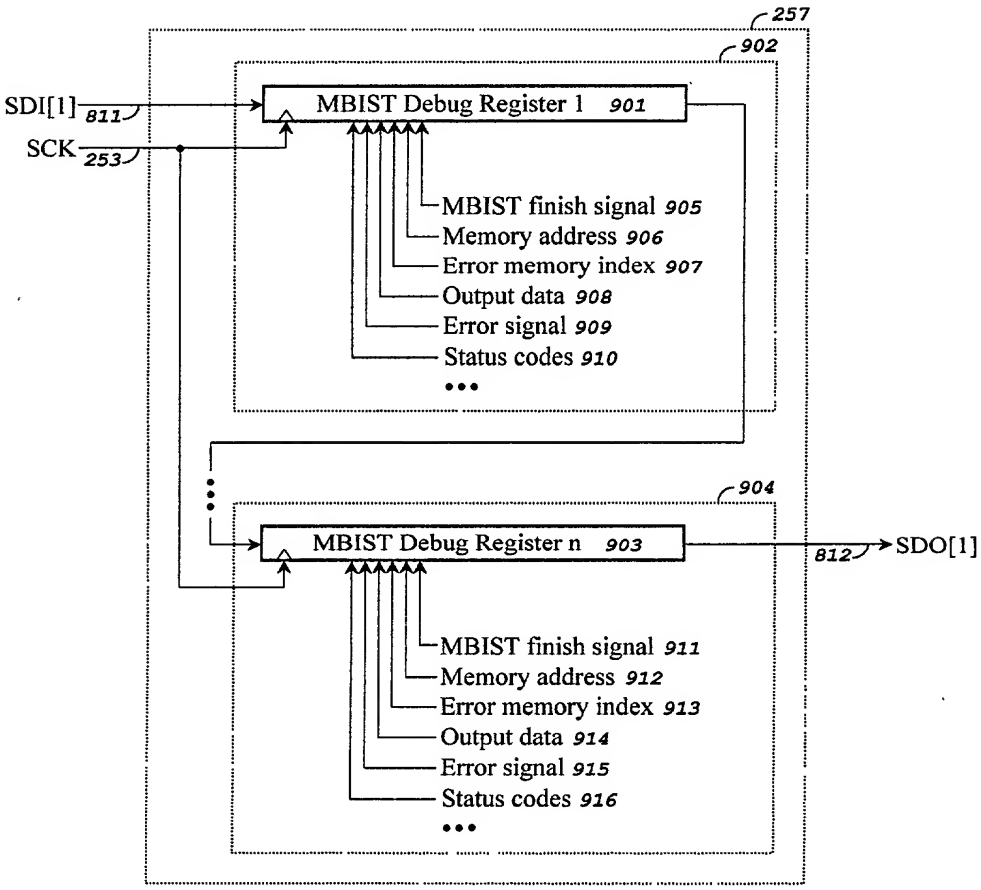

257
902
SDI[1]
811
SCK
253
MBIST Debug Register 1 901
MBIST finish signal 905
Memory address 906
Error memory index 907
Output data 908
Error signal 909
Status codes 910
904
MBIST Debug Register n 903
812
SDO[1]
MBIST finish signal 911
Memory address 912
Error memory index 913
Output data 914
Error signal 915
Status codes 916

FIG. 9

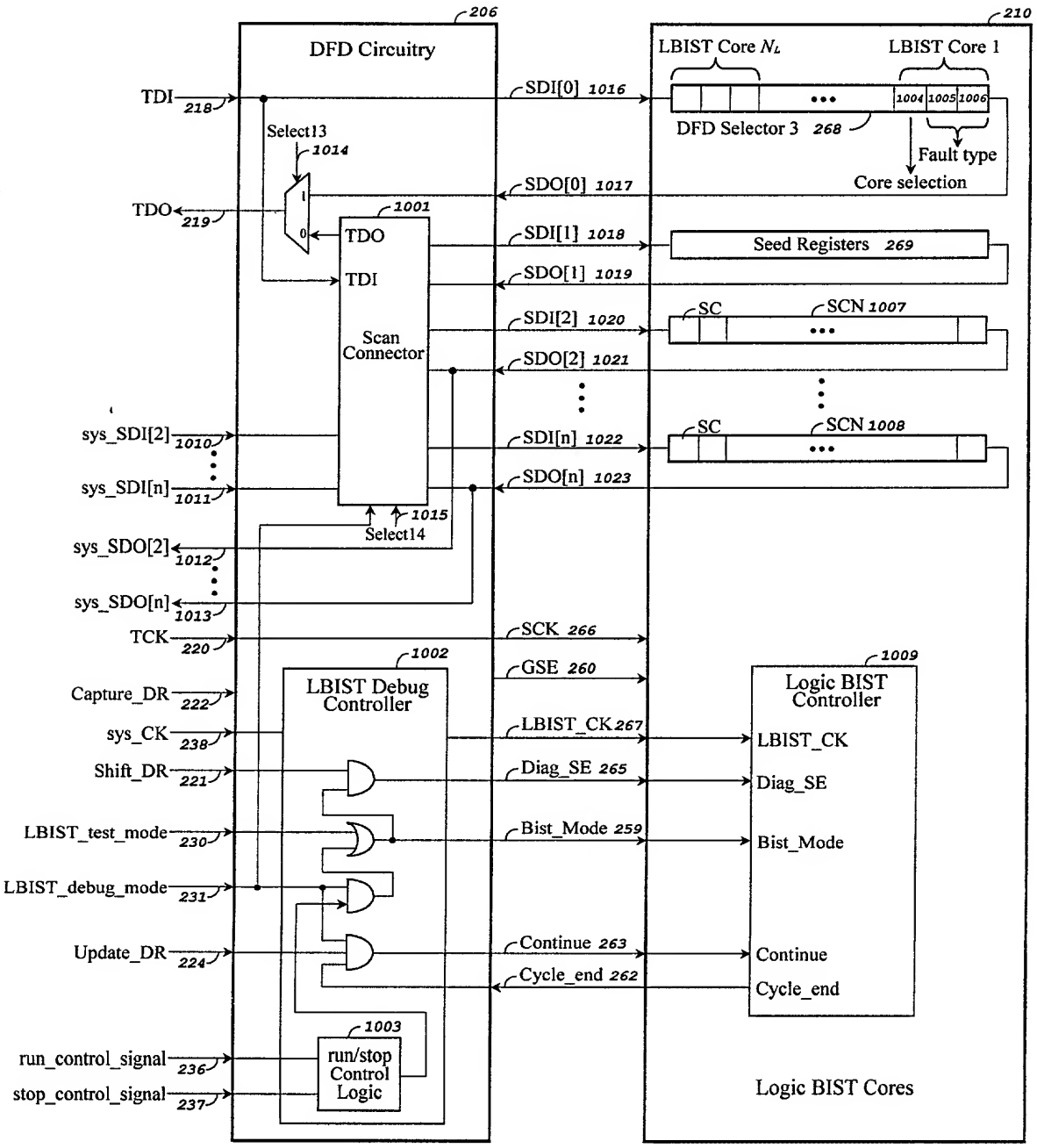

206
DFD Circuitry
210
LBIST Core N_L
LBIST Core 1
TDI 218
SDI[0] 1016
1004
1005
1006
DFD Selector 3 268
Fault type
Core selection
Select13 1014
SDO[0] 1017
TDO 219
1001
TDO
TDI
Scan Connector
SDI[1] 1018
Seed Registers 269
SDO[1] 1019
SDI[2] 1020
SC
SCN 1007
SDO[2] 1021
sys_SDI[2] 1010
SDI[n] 1022
SC
SCN 1008
sys_SDI[n] 1011
SDO[n] 1023
1015
Select14
sys_SDO[2] 1012
sys_SDO[n] 1013
TCK 220
SCK 266
1002
LBIST Debug Controller
1009
Logic BIST Controller
Capture_DR 222
GSE 260
sys_CK 238
LBIST_CK 267
LBIST_CK
Shift_DR 221
Diag_SE 265
Diag_SE
LBIST_test_mode 230
Bist_Mode 259
Bist_Mode
LBIST_debug_mode 231
Update_DR 224
Continue 263
Continue
Cycle_end 262
Cycle_end
1003
run/stop Control Logic
run_control_signal 236
stop_control_signal 237
Logic BIST Cores

FIG. 10

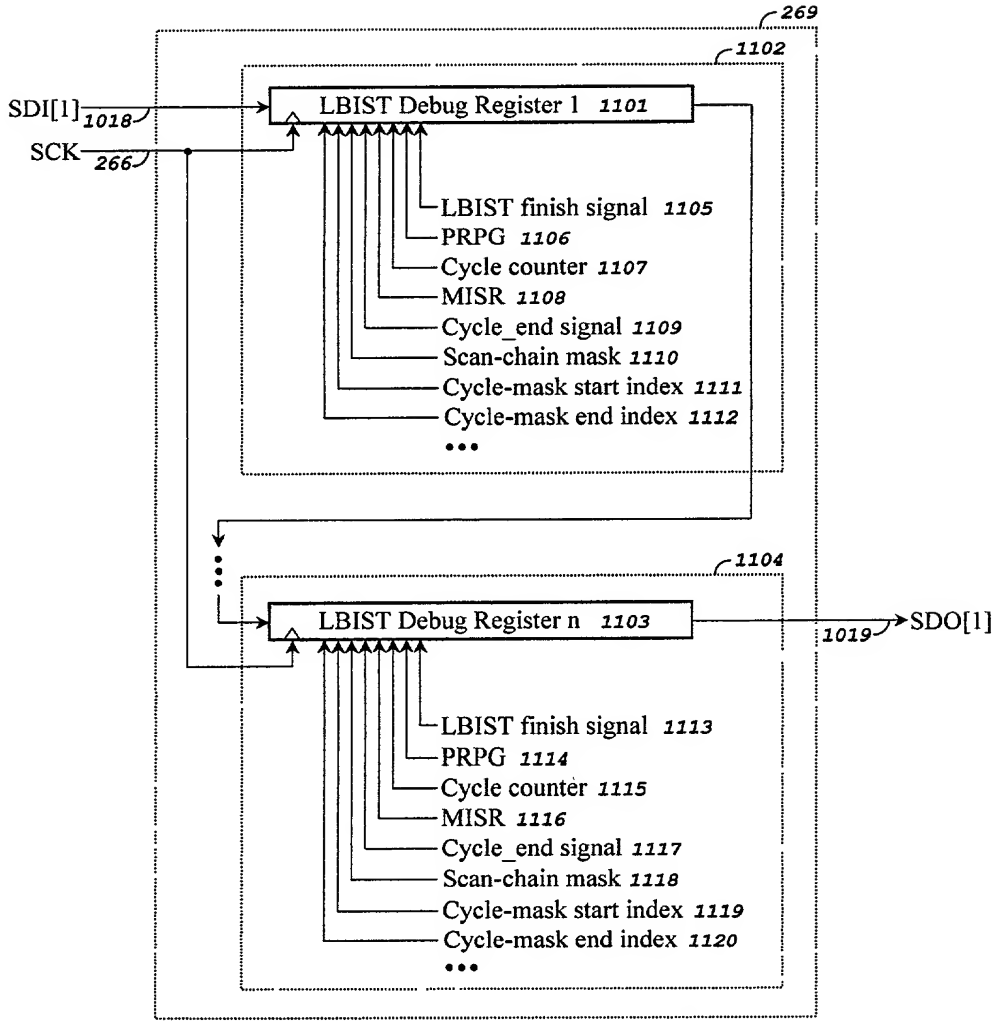

269
1102
SDI[1]
1018
SCK
266
LBIST Debug Register 1 1101
LBIST finish signal 1105
PRPG 1106
Cycle counter 1107
MISR 1108
Cycle_end signal 1109
Scan-chain mask 1110
Cycle-mask start index 1111
Cycle-mask end index 1112
1104
LBIST Debug Register n 1103
1019
SDO[1]
LBIST finish signal 1113
PRPG 1114
Cycle counter 1115
MISR 1116
Cycle_end signal 1117
Scan-chain mask 1118
Cycle-mask start index 1119
Cycle-mask end index 1120

FIG. 11

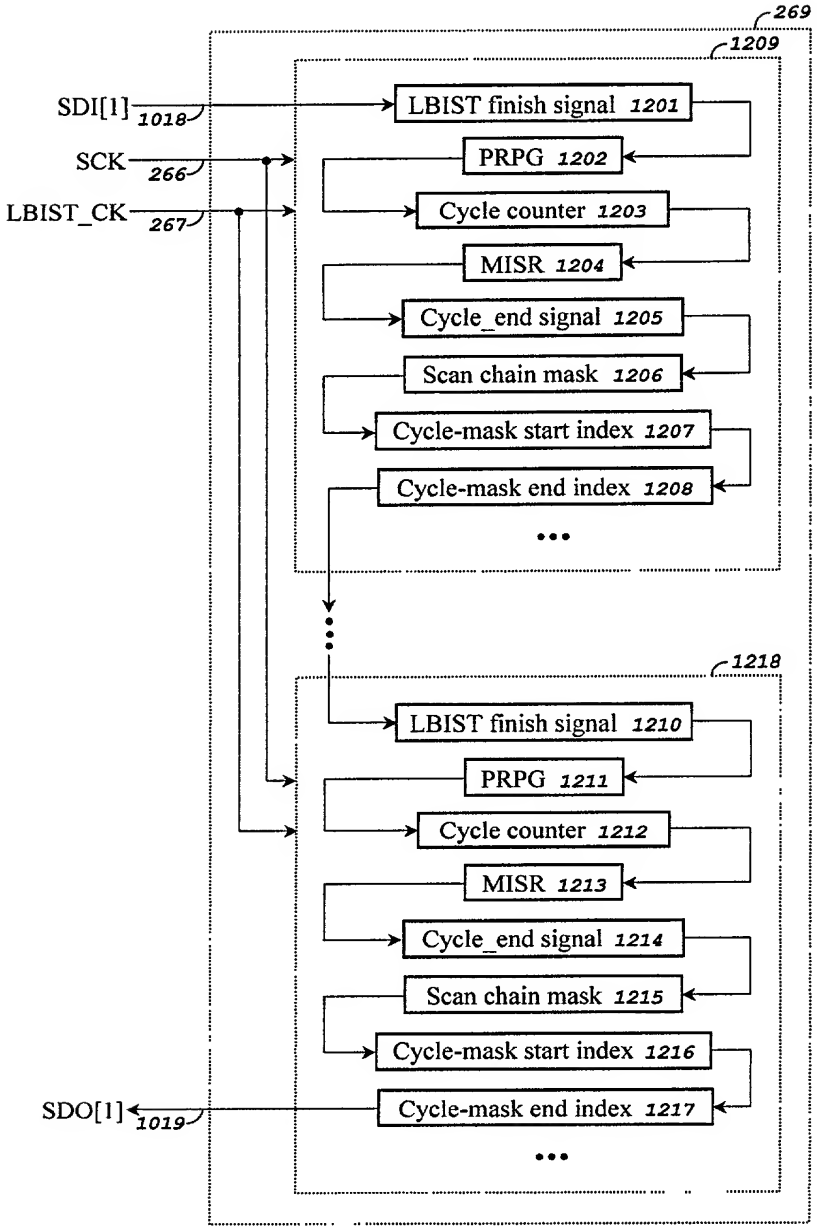

269
1209
SDI[1]
1018
SCK
266
LBIST_CK
267
LBIST finish signal 1201
PRPG 1202
Cycle counter 1203
MISR 1204
Cycle_end signal 1205
Scan chain mask 1206
Cycle-mask start index 1207
Cycle-mask end index 1208
1218
LBIST finish signal 1210
PRPG 1211
Cycle counter 1212
MISR 1213
Cycle_end signal 1214
Scan chain mask 1215
Cycle-mask start index 1216
Cycle-mask end index 1217
SDO[1]
1019

FIG. 12

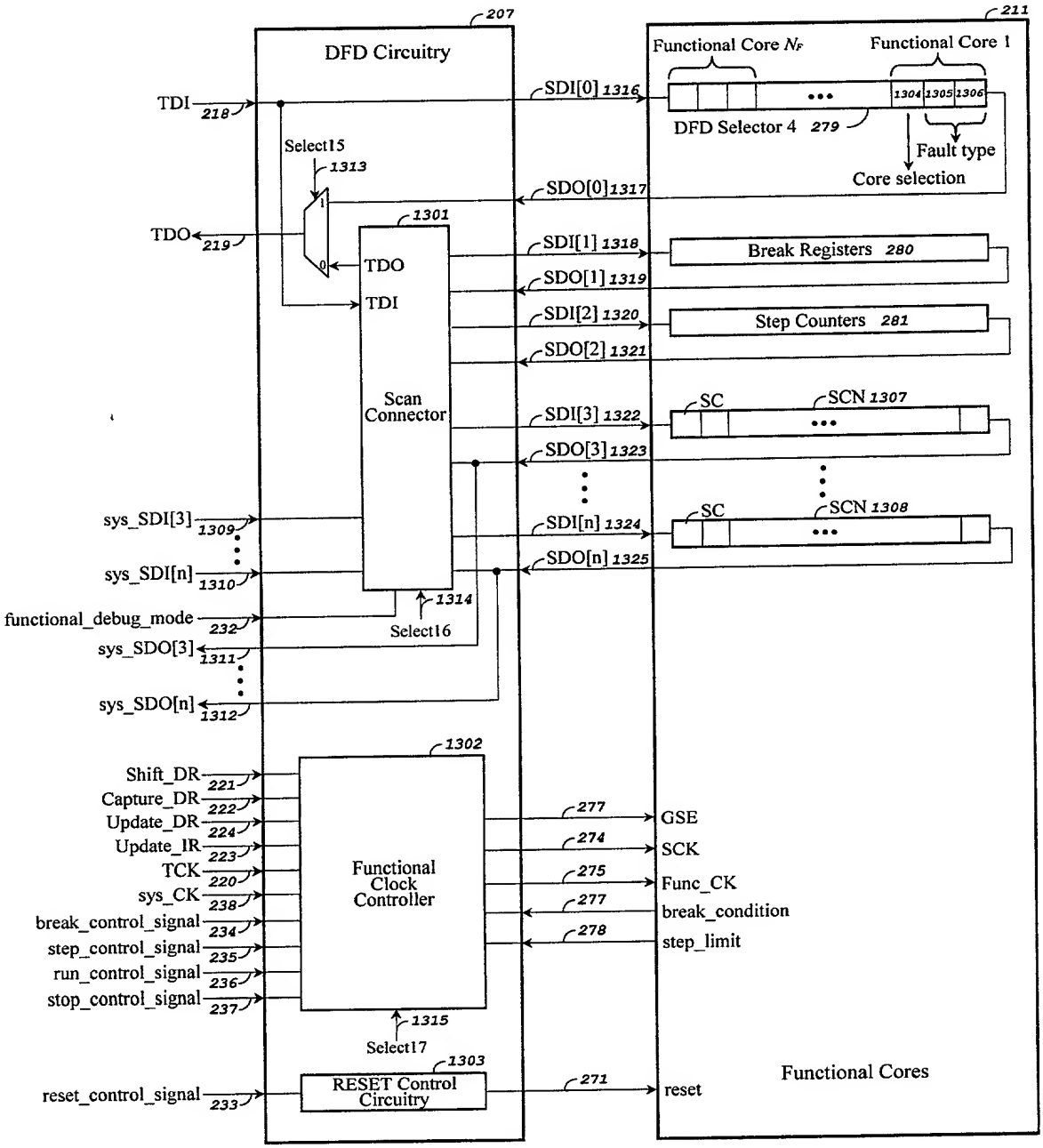

207
DFD Circuitry
211
Functional Core N_F
Functional Core 1
TDI 218
SDI[0] 1316
1304 1305 1306
DFD Selector 4 279
Fault type
Core selection
Select15
1313
SDO[0] 1317
TDO 219
1301
TDO
TDI
SDI[1] 1318
Break Registers 280
SDO[1] 1319
SDI[2] 1320
Step Counters 281
SDO[2] 1321
Scan Connector
SC
SCN 1307
SDI[3] 1322
SDO[3] 1323
SC
SCN 1308
SDI[n] 1324
SDO[n] 1325
sys_SDI[3] 1309
sys_SDI[n] 1310
functional_debug_mode 232
1314
Select16
sys_SDO[3] 1311
sys_SDO[n] 1312
1302
Shift_DR 221
Capture_DR 222
Update_DR 224
Update_IR 223
TCK 220
sys_CK 238
break_control_signal 234
step_control_signal 235
run_control_signal 236
stop_control_signal 237
Functional Clock Controller
277
GSE
274
SCK
275
Func_CK
277
break_condition
278
step_limit
1315
Select17
1303
RESET Control Circuitry
reset_control_signal 233
271
reset
Functional Cores

FIG. 13

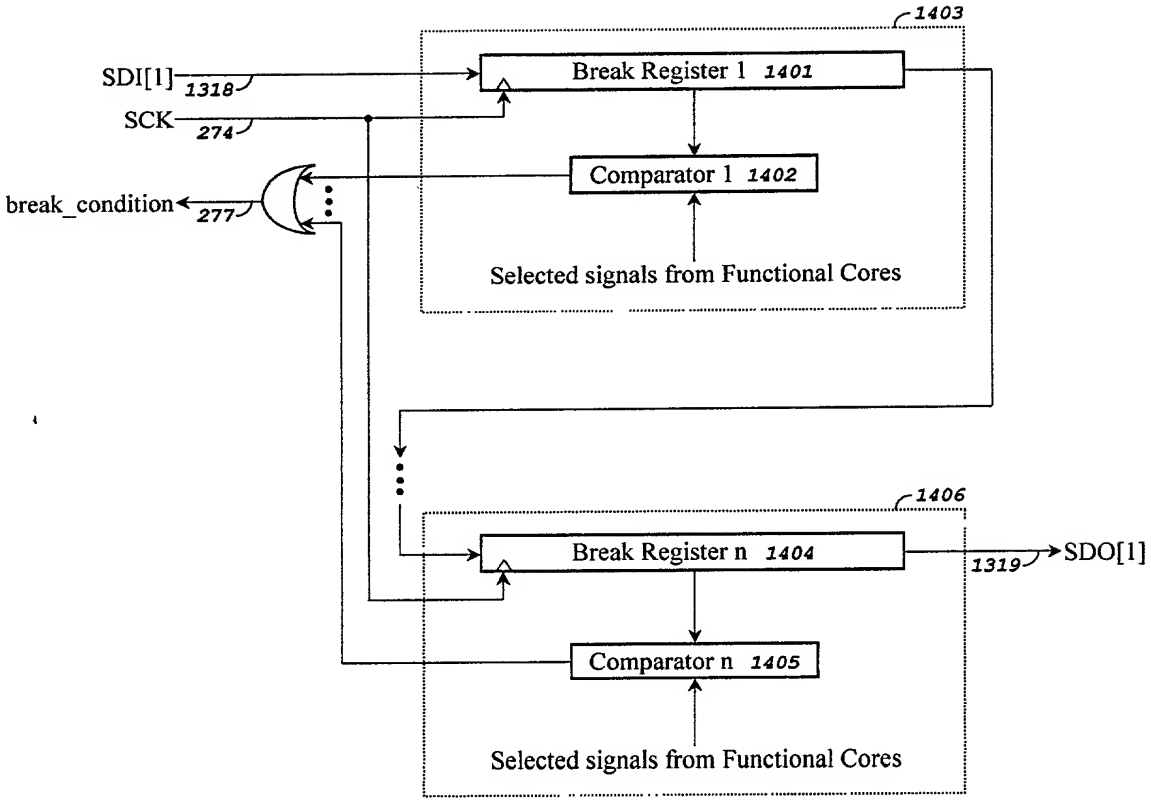

1403
SDI[1]
1318
SCK
274
Break Register 1 1401
Comparator 1 1402
break_condition
277
Selected signals from Functional Cores
1406
Break Register n 1404
1319
SDO[1]
Comparator n 1405
Selected signals from Functional Cores

FIG. 14

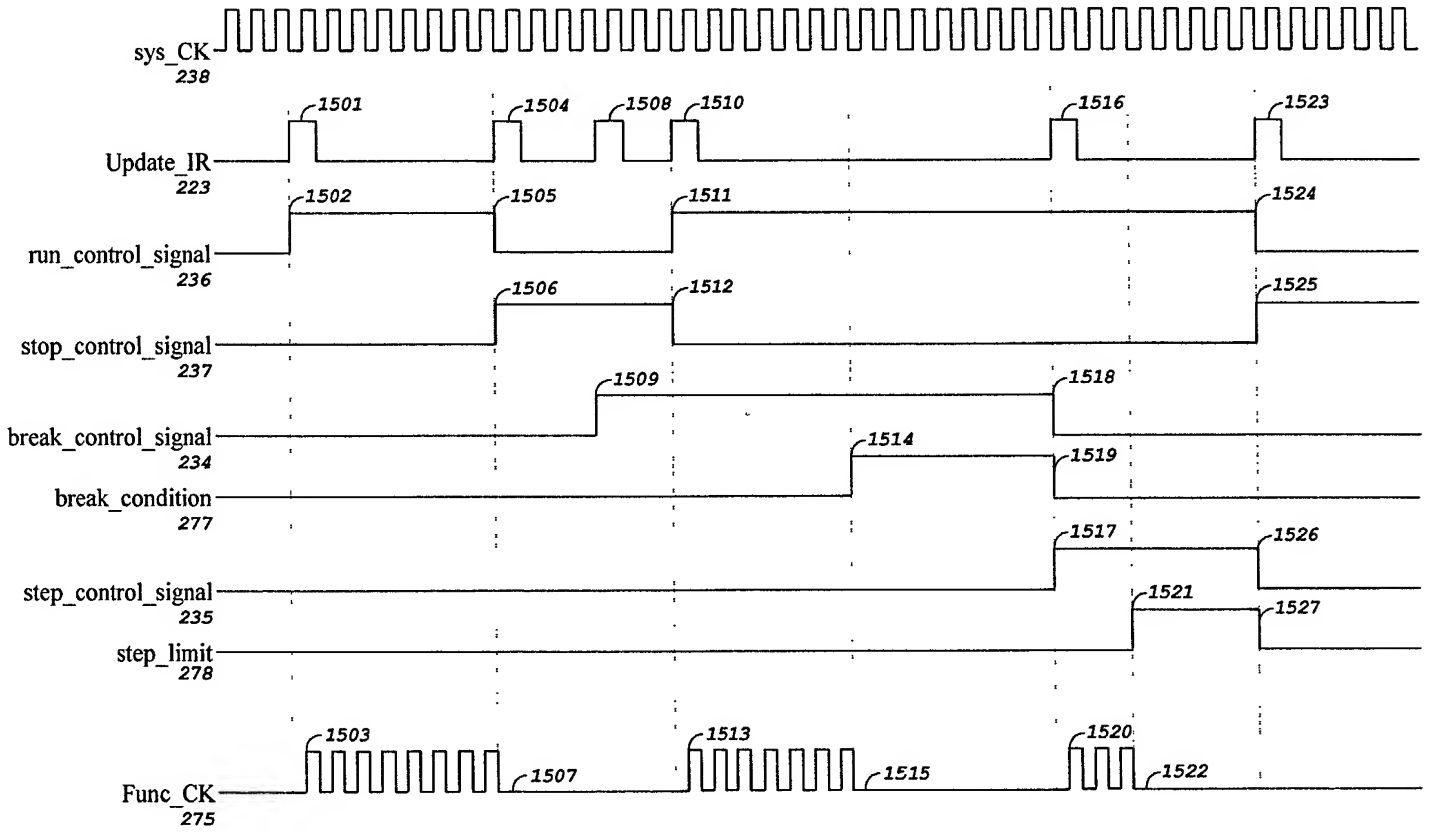

sys_CK
238
Update_IR
223
run_control_signal
236
stop_control_signal
237
break_control_signal
234
break_condition
277
step_control_signal
235
step_limit
278
Func_CK
275
1501
1504
1508
1510
1516
1523
1502
1505
1511
1524
1506
1512
1525
1509
1518
1514
1519
1517
1526
1521
1527
1503
1507
1513
1515
1520
1522

FIG. 15

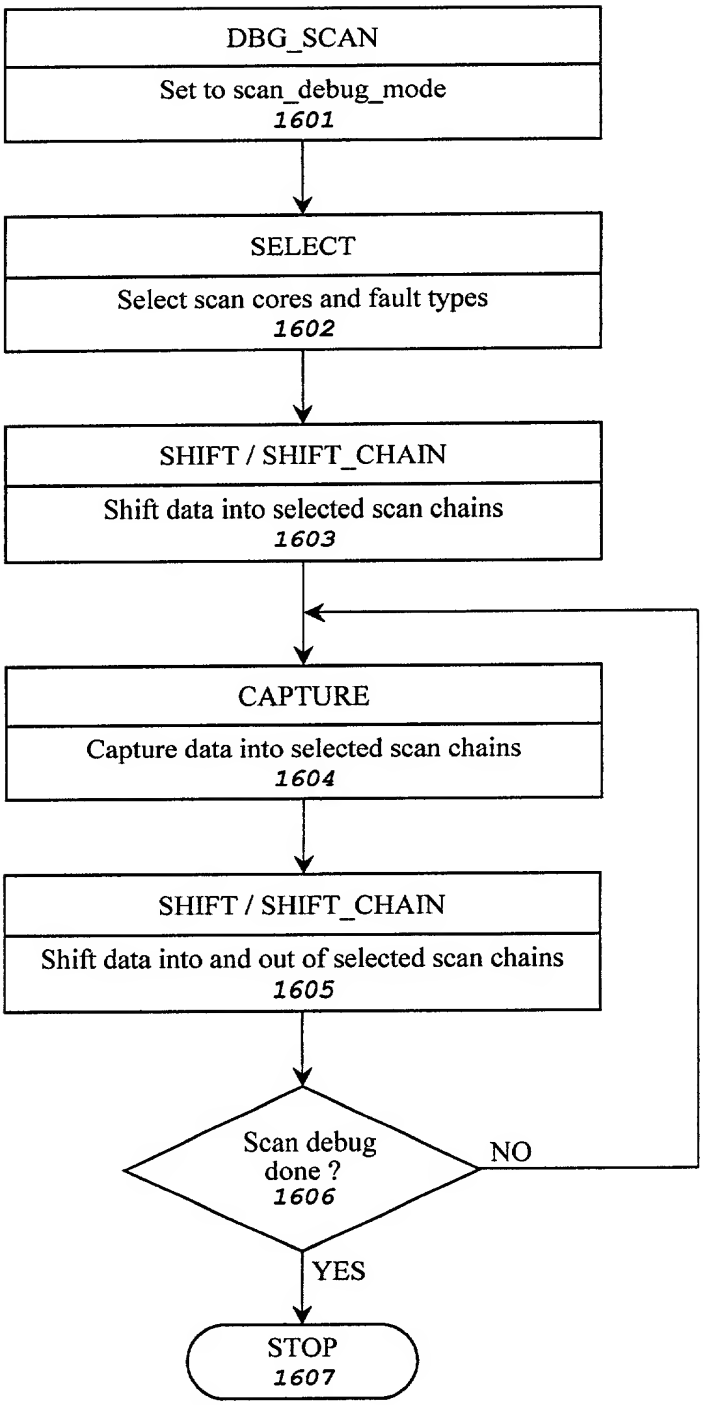

DBG_SCAN
Set to scan_debug_mode
1601
SELECT
Select scan cores and fault types
1602
SHIFT / SHIFT_CHAIN
Shift data into selected scan chains
1603
CAPTURE
Capture data into selected scan chains
1604
SHIFT / SHIFT_CHAIN
Shift data into and out of selected scan chains
1605
Scan debug done ?
1606
NO
YES
STOP
1607

FIG. 16

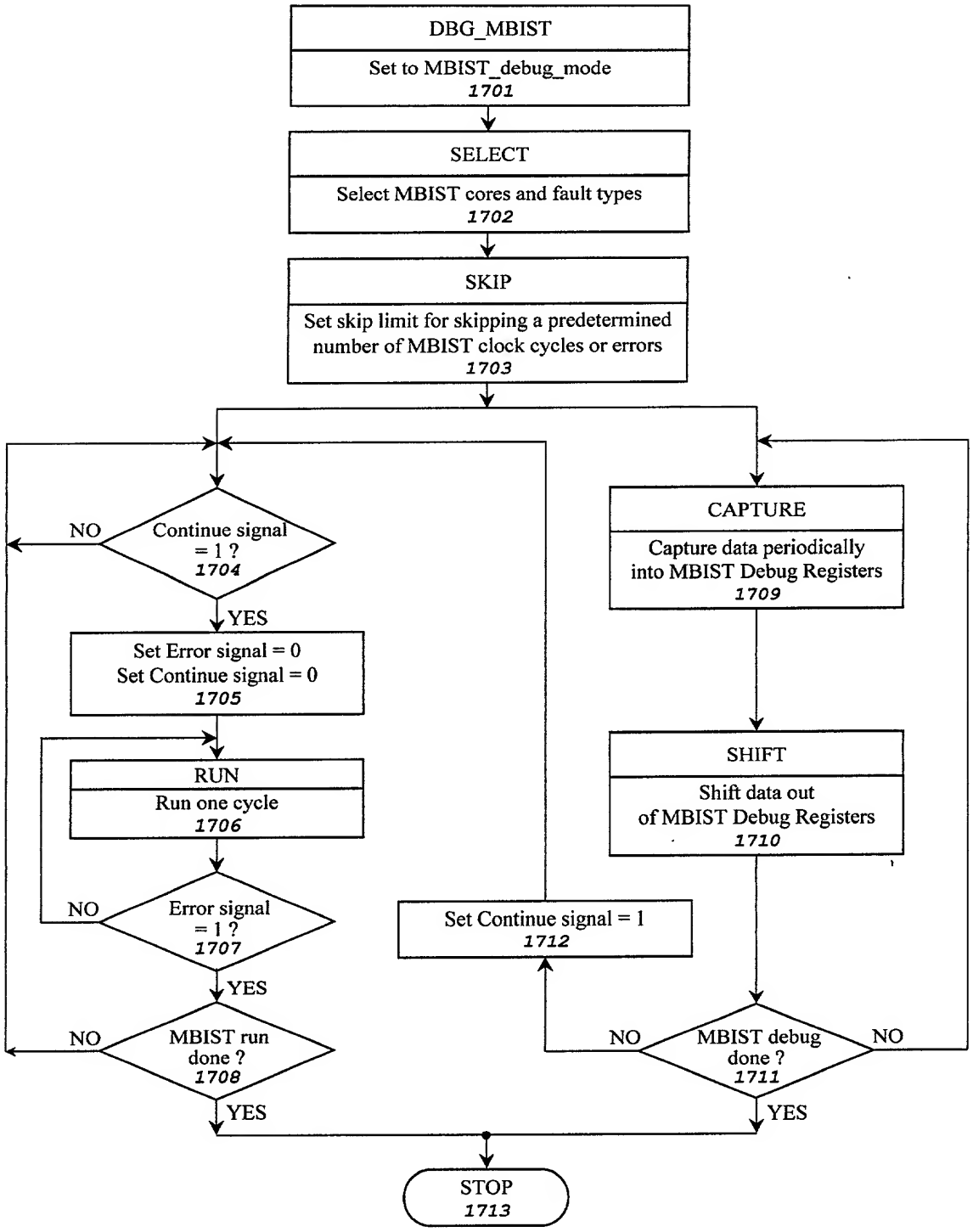

DBG_MBIST
Set to MBIST_debug_mode
1701
SELECT
Select MBIST cores and fault types
1702
SKIP
Set skip limit for skipping a predetermined number of MBIST clock cycles or errors
1703
Continue signal = 1 ?
1704
NO
YES
Set Error signal = 0
Set Continue signal = 0
1705
RUN
Run one cycle
1706
Error signal = 1 ?
1707
NO
YES
MBIST run done ?
1708
NO
YES
CAPTURE
Capture data periodically into MBIST Debug Registers
1709
SHIFT
Shift data out of MBIST Debug Registers
1710
Set Continue signal = 1
1712
MBIST debug done ?
1711
NO
NO
YES
STOP
1713

FIG. 17

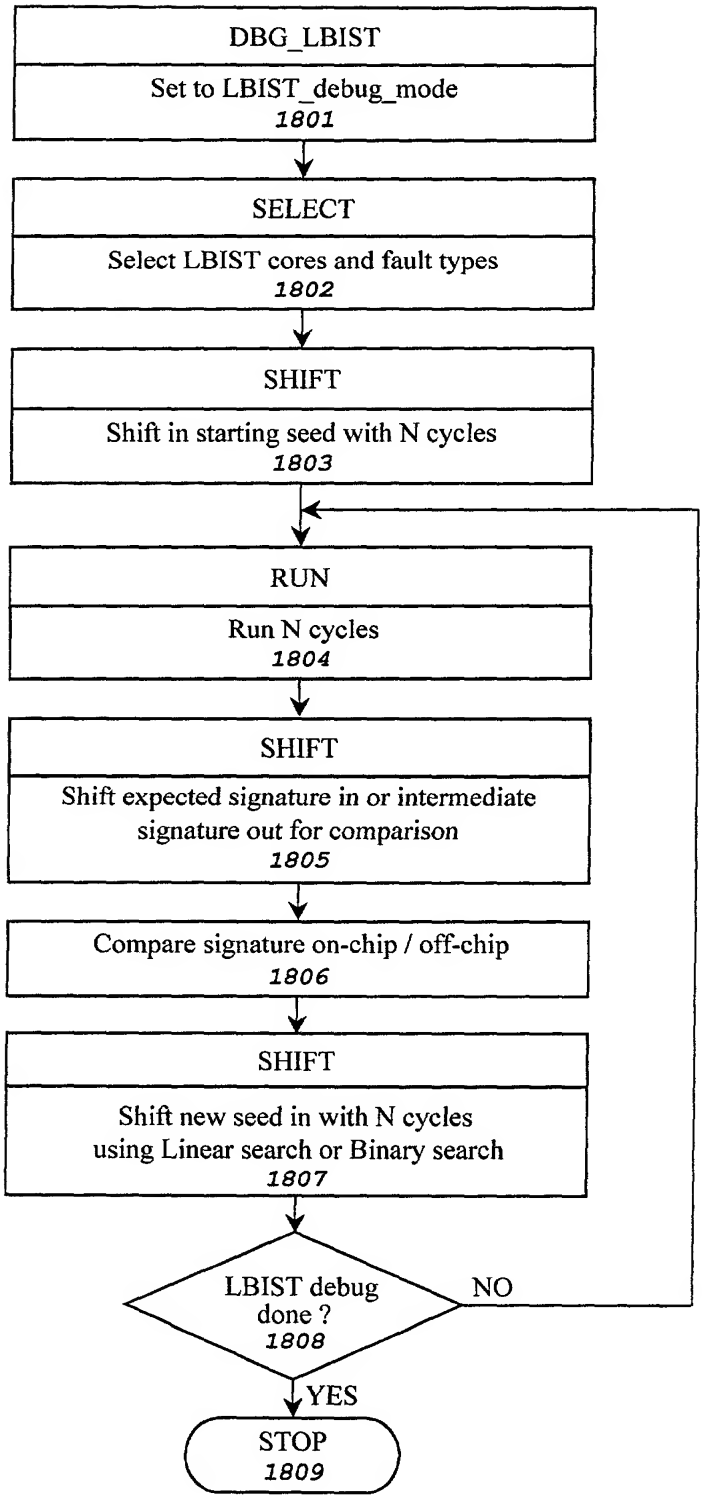

DBG_LBIST
Set to LBIST_debug_mode
1801
SELECT
Select LBIST cores and fault types
1802
SHIFT
Shift in starting seed with N cycles
1803
RUN
Run N cycles
1804
SHIFT
Shift expected signature in or intermediate signature out for comparison
1805
Compare signature on-chip / off-chip
1806
SHIFT
Shift new seed in with N cycles using Linear search or Binary search
1807
LBIST debug done ?
1808
NO
YES
STOP
1809

FIG. 18

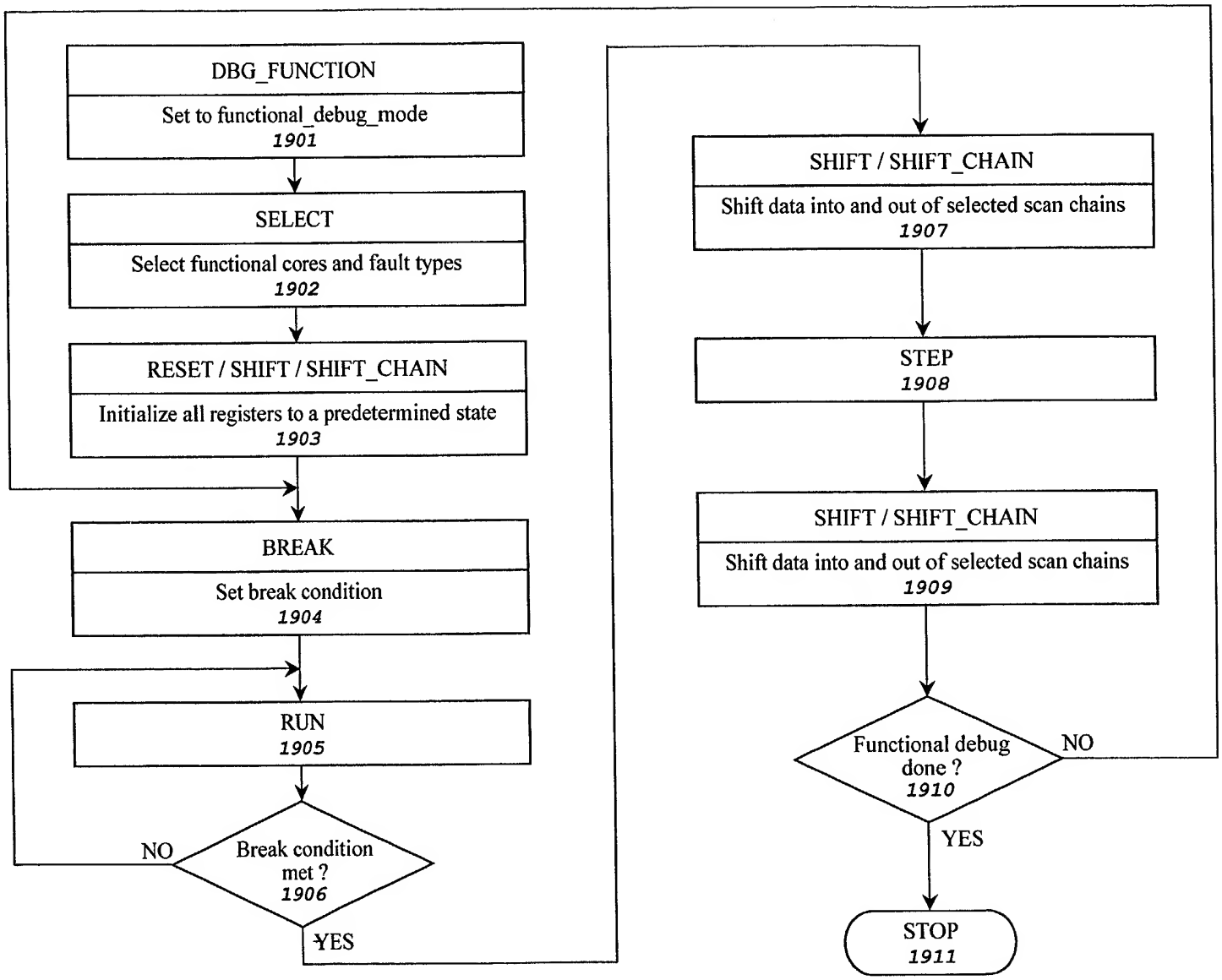

DBG_FUNCTION
Set to functional_debug_mode
1901
SELECT
Select functional cores and fault types
1902
RESET / SHIFT / SHIFT_CHAIN
Initialize all registers to a predetermined state
1903
BREAK
Set break condition
1904
RUN
1905
Break condition met ?
1906
NO
YES
SHIFT / SHIFT_CHAIN
Shift data into and out of selected scan chains
1907
STEP
1908
SHIFT / SHIFT_CHAIN
Shift data into and out of selected scan chains
1909
Functional debug done ?
1910
NO
YES
STOP
1911

FIG. 19

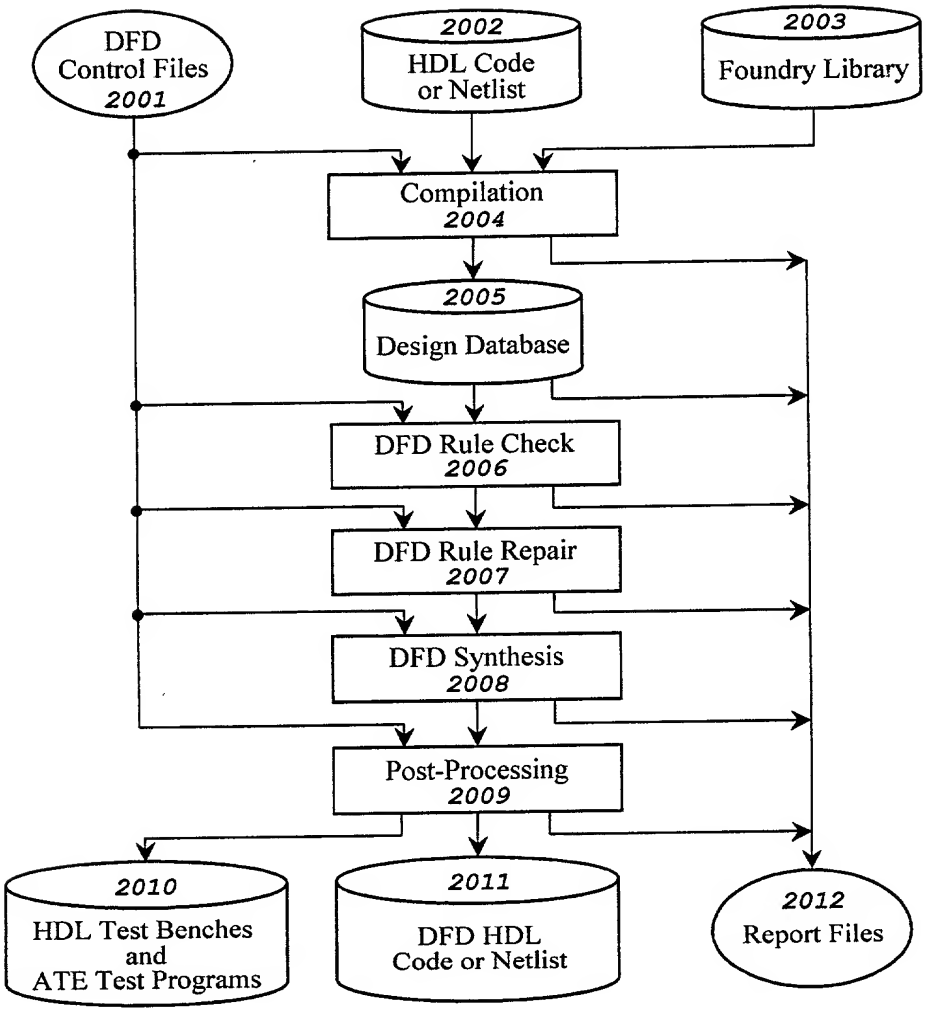

DFD
Control Files
2001
2002
HDL Code
or Netlist
2003
Foundry Library
Compilation
2004
2005
Design Database
DFD Rule Check
2006
DFD Rule Repair
2007
DFD Synthesis
2008
Post-Processing
2009
2010
HDL Test Benches
and
ATE Test Programs
2011
DFD HDL
Code or Netlist
2012
Report Files

FIG. 20